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Formation of polycrystalline silicon germanium/HfO_2 gate stack structure using inductively coupled plasma etching

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A gate stack structure consisting of a polycrystalline silicon germanium (poly-SiGe) conductor and a HfO_2 dielectric on a silicon substrate was formed by inductively coupled plasma etching using $HBr/Cl_2/O_2$. Etch rates of poly-SiGe with 46% Ge were 1.7–2.0 times higher than those of polycrystalline silicon, depending on processing conditions. In the small feature sized devices of 100 nm gates, the notching at the sidewall of poly-SiGe was pronounced up to the depth of 50 nm. The amount of notching increased with increasing inductive power and pressure, and decreasing rf bias power. A HfO_2 etch rate of 950 Å/min was obtained at the condition of 550 W inductive power, 360 W rf bias power, and 10 mTorr pressure. Etch rates of HfO_2 increased with increasing inductive power and rf bias power. Etching selectivity of poly-SiGe with respect to HfO_2 increased significantly with the addition of 3.8% O_2 to HBr, and it was possible to control the selectivity in the range of 15–70 by changing the rf bias power. The change in etching selectivity was considered mainly due to the change in HfO_2 film property, originating from the incorporation of O into the remaining nonvolatile Hf and the reformation of HfO_x during etching. © *2003 American Vacuum Society.* [DOI: 10.1116/1.1586283]

I. INTRODUCTION

As complementary metal–oxide–semiconductor (CMOS) technology is further scaled into the deep submicron region, materials need to be considered which can deliver performance enhancements beyond that realized in current technology. This is seen in the development of high dielectric constant (high-*k*) materials for the gate stack and low-*k* materials for the interconnect. Single crystalline silicon germanium (SiGe) has been extensively investigated as a material for the CMOS device channel which can provide higher carrier mobility.[1,2] Polycrystalline SiGe (poly-SiGe), on the other hand, is found to have several advantages as a suitable gate conducting material to replace polycrystalline silicon (poly-Si). Poly-SiGe gates have been found to be useful in reducing polycrystalline depletion and boron penetration effects,[3] and with adjusted Ge concentrations, can provide different work functions suitable for a *p*-channel device.[4,5]

Reports have been made regarding the etching of poly-SiGe material using reactive ion etching (RIE) techniques.[6–9] The common finding in these cases is that the etch rate of poly-SiGe increases with Ge concentration. Oehrlein *et al.*[10] reported that the experimental etch rates were greater than those from their proposed models and gave a thorough discussion to explain this phenomenon. They reported that the increase in the etch rate could not be accounted for by the greater gasification of Ge atoms alone, but that the presence of Ge atoms in the SiGe alloy increased the rate of the Si etch products formation. Several reasons were proposed. They believed that the availability of electrons at the surface is important in explaining the increased etch rate, and this is similar to the "doping effect" in Si where the etch rate changes with the type and amount of dopants used. Furthermore, the surface of SiGe was found to become richer in Ge when using CF_4, while on the other hand, it became richer in Si when using CF_2Cl_2 or HBr. Cheung *et al.*[11] reported that the etch rate and etch profile of $Si_{0.75}Ge_{0.25}$ were strongly influenced by the substrate temperature and the oxygen content in the $SF_6/O_2/He$ gas mixture. There was also a report[7] indicating that the difference in the enrichment was highly dependent on ion bombardment, and preferential sputtering was cited as the most plausible mechanism.

Etching of semiconductor materials has moved from the conventional RIE system to a system using a higher plasma density. In a study of etching SiGe in high-density plasmas, Vallon *et al.*[12] showed that the recipe previously developed for the etching of Si was unsuitable for etching SiGe, with the etch profile being affected when a helicon source was used. This effect also depended significantly on the Ge concentration in SiGe. A surface study on SiGe using x-ray photoelectron spectroscopy (XPS) was also performed by them in another work.[13] Etching of SiGe using an electron cyclotron resonance source[7] was also investigated to determine the effect of ion bombardment on surface stoichiometry as mentioned previously. In our work, the dependence of etch profiles and etch rates on process parameters is studied to understand etching mechanisms of poly-SiGe when using an inductively coupled plasma (ICP) source.

After completing the dry etching process of the poly-SiGe gate conductor, the underlying thin gate dielectric is usually removed by diluted HF, since wet etching of dielectric films using concentrated HF results in significant undercutting. According to recent reports,[14,15] wet etch rates of high-*k*

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films as gate dielectrics are extremely low, particularly after they have been annealed. Developing a suitable process for the dry etching of HfO_2 is a challenge that needs to be overcome before the material can be incorporated into advanced gate stacks. Exploiting the difficulty for HfO_2 to form volatile products during plasma etching, there have been reports[16,17] of using the HfO_2 film as an etch-stop layer. Recently, Norasetthekul *et al.*[18] reported on the etching of HfO_2 films in an ICP etcher using Cl_2 and SF_6.

In this article, we report on results obtained from ICP etching of poly-SiGe and HfO_2 with the aim of forming poly-SiGe/high-k gate stacks using industry compatible etching equipment. We also demonstrate the formation of controlled notches from the poly-SiGe sidewall as a step toward the development of short channel devices with a technology node smaller than 65 nm.

II. EXPERIMENTAL DETAILS

The samples used in this work were prepared by a gate cluster system manufactured by Jusung Engineering Co. The system consists of three processing modules for metalorganic chemical vapor deposition (MOCVD) of high-k dielectrics, chemical vapor deposition (CVD) of poly-SiGe deposition, and postdeposition annealing, respectively. In the gate cluster system, these processing steps are carried out in sequence without breaking the vacuum. All the poly-Si and poly-SiGe films were deposited by CVD using SiH_4 and GeH_4 at a temperature of 550 °C and a pressure of 5 Torr. The SiH_4 flow rate was fixed at 60 sccm, but the GeH_4 flow rate was varied from 0 to 200 sccm to obtain various Ge concentrations in poly-SiGe. The Ge concentrations of poly-SiGe samples used in this study were 15%, 23%, 32%, and 46%, and these were determined using Rutherford backscattering spectrometry (RBS). The poly-Si and poly-SiGe films in the thickness range from 500 to 3000 Å were deposited either on SiO_2 thermally grown from the oxidation furnace or on 60 Å thick HfO_2 grown from the MOCVD module of the gate–cluster system. The 400 Å thick HfO_2 films were also prepared for the measurement of the etch rates of HfO_2 and the etching selectivities of poly-SiGe with respect to HfO_2. The SiO_2 films were grown on 6 in. Si wafers at a temperature of 1030 °C with O_2 at atmospheric pressure. The HfO_2 films were deposited on 6 in. Si wafers using the $Hf[OC(CH_3)_3]_4$ precursor at 400 °C with 50 sccm O_2 and 100 sccm Ar. The deposition pressure was fixed at 400 mTorr. After the deposition, the annealing process was carried out at 700 °C for 1 min in a N_2 ambient.

The thicknesses of blanket films were determined by an ellipsometer. Etch rates and selectivities were determined by measuring the etching times and etched thicknesses. The etched thicknesses of the films patterned by a 0.6 μm gate mask were determined by a surface profiler. The etch rates obtained from the blanket films and the patterned films were about the same to within the range of measurement error. The 0.6 μm gate patterns were also used for cross-sectional scanning electron microscopy (SEM) observations of poly-SiGe. The test patterns of 0.13 μm were used for investigating the etched profile of gate stacks of gate length below 0.1 μm by TEM.

All the poly-Si and poly-SiGe samples were etched using the ICP etching module (TCP 9400SE manufactured by Lam Research Co.). The wafer is electrostatically clamped to the bottom rf electrode and cooled by He flowing through between the back side of the wafer and the grooved electrode. The temperature of the wafer electrode and the chamber wall was maintained at 60 °C. Reactant feed gases were introduced into the chamber from the bottom. In this study, various gas combinations of $HBr/Cl_2/O_2$ were used for each of the following four etching steps for the gate stack: Breakthrough etching of poly-SiGe, main etching of poly-SiGe, overetching of poly-SiGe, and etching of HfO_2. Studies on the etching of HfO_2 with $HBr/Cl_2/O_2$ plasmas were performed using the TCP9400SE, whereas studies on the HfO_2 etching with CF_4 plasmas were performed using another etcher (ICP2) of similar configuration to the TCP9400SE. Differences of the ICP2 from the TCP9400SE are as follows: (1) ICP2 uses the step on the electrode and gravity to hold the wafer, whereas the TCP9400SE uses an electrostatic chuck, (2) inductive power is supplied via a 5.75 turn coil for the ICP2, whereas it is supplied via a four-turn coil for the TCP9400SE, and (3) gases are introduced from the sidewall inlets for the ICP2, whereas they are introduced from the bottom inlets for the TCP9400SE. To investigate the etching characteristics at various conditions, the processing parameters were varied in the following ranges: 200 to 550 W for inductive power, 0 to 360 W for rf bias power, and 10 to 80 mTorr for pressure.

Optical emission was monitored to investigate the property of the plasma species during the etching of the poly-SiGe/HfO_2 gate stack on the Si substrate. Optical emission spectra in the wavelength range of 200 to 800 nm were collected using a charge coupled device spectrograph via an optical fiber fixed on the sidewall of the reactor. Also, the temporal change in the intensity of the fixed emission spectra was monitored during the gate stack etching.

III. RESULTS

A. Etching of polycrystalline silicon germanium

Figures 1(a)–1(c) summarize the etch rates obtained by varying in turn the inductive power, rf bias power, and pressure, using the baseline recipe of an inductive power of 550 W, an rf bias power of 200 W, a pressure of 10 mTorr, and a HBr flow of 200 sccm. From the baseline condition, we obtained the etch rates of 2660 Å/min for poly-Si and 5270 Å/min for poly-$Si_{0.54}Ge_{0.46}$. From Fig. 1, it can be observed that the etch rate of poly-SiGe increases approximately linearly with increasing Ge concentration, although the slight deviation toward the high etch rate was observed at 46% Ge. Models were suggested by Oherlein *et al.* in RIE[10] to explain the deviation from the linear relation, but their experimental results did not quite agree with their models. As shown in Fig. 1, the etch rates were affected by changing the process parameters: 2040–4080 Å/min for the 250 W inductive

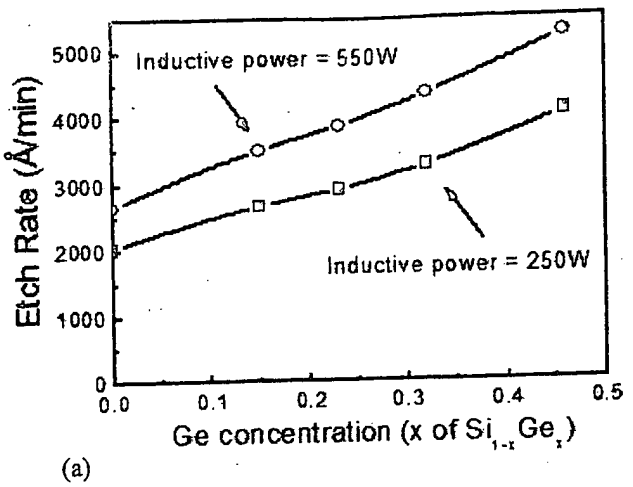


FIG. 1. Poly-SiGe etch rates as a function of Ge concentration at the different (a) inductively powers, (b) rf bias powers, and (c) pressures (parameters are fixed otherwise at inductive power of 550 W, rf bias power of 200 W, pressure of 10 mTorr, and HBr flow of 200 sccm).

power, 2030–3390 Å/min for the 40 W rf bias power, and 1960–3640 Å/min for the 80 mTorr pressure. However, the trend of the linear increase of etching rates with increasing Ge concentration remained unchanged.

Figure 2 shows etch rates as a function of pressure from 10 mTorr to 80 mTorr for different Ge concentrations. A peak

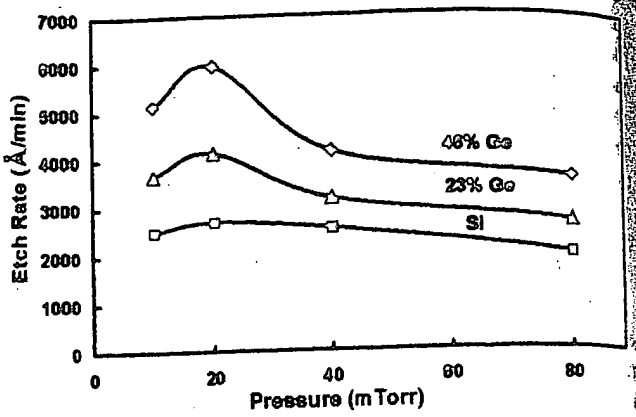


FIG. 2. Etch rates of poly-Si, poly-$Si_{0.77}Ge_{0.23}$, and poly-$Si_{0.54}Ge_{0.46}$ as a function of pressure (inductive power: 550 W, rf bias power: 200 W, and gas flow: HBr 200 sccm).

value for the poly-SiGe etch rates is observed at around 20 mTorr. A similar trend was reported in RIE by Zhang *et al.*,[7] but the peak was observed at around 75 mTorr in their work. The trend is more obvious for samples with the larger Ge concentration. Figures 3(a) and 3(b) show the etch rates as a function of rf bias power at 10 mTorr and 80 mTorr for poly-SiGe samples for various Ge concentrations. It was found that, as the rf bias power increased, the etch rates

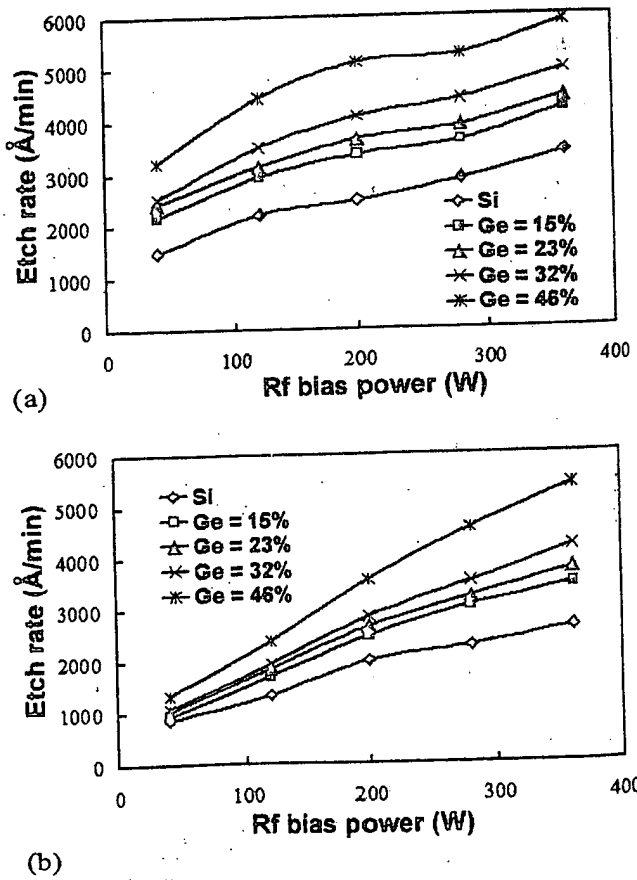


FIG. 3. Poly-SiGe etch rates as a function of rf bias power at (a) 10 mTorr and (b) 80 mTorr.

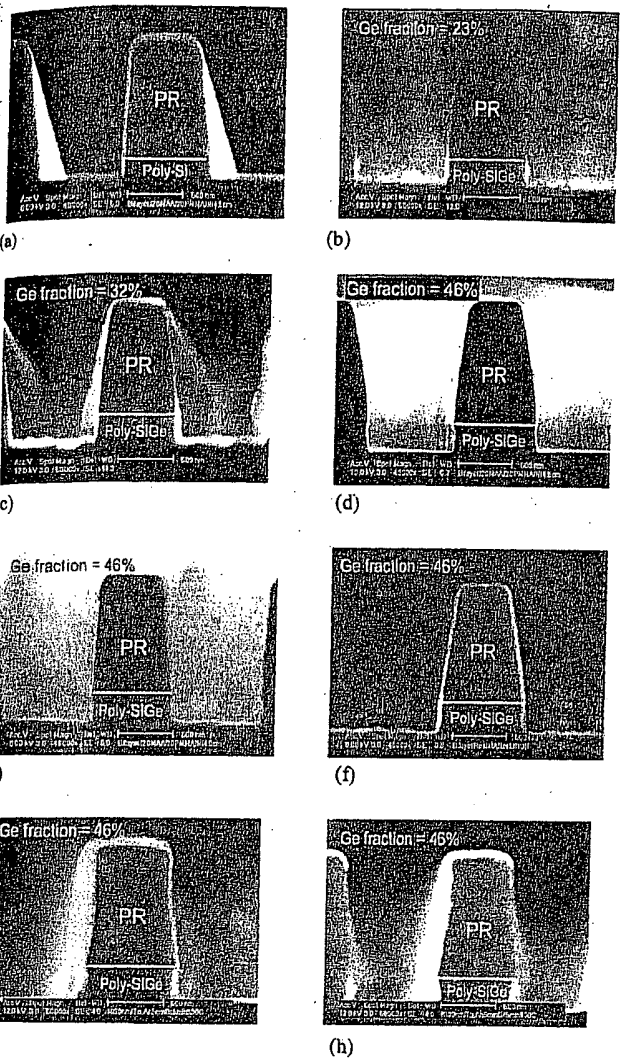


FIG. 4. SEM of etching profiles for (a) poly-Si, (b) poly-$Si_{0.77}Ge_{0.23}$, (c) poly-$Si_{0.68}Ge_{0.32}$, (d) poly-$Si_{0.54}Ge_{0.46}$, (e) poly-$Si_{0.54}Ge_{0.46}$ (pressure: 10 mTorr), (f) poly-$Si_{0.54}Ge_{0.46}$ (rf bias power: 280 W), (g) poly-$Si_{0.54}Ge_{0.46}$ (inductive power: 250 W), and (h) poly-$Si_{0.54}Ge_{0.46}$ (inductive power: 550 W). [(a)–(f): Parameters are fixed otherwise at inductive power of 550 W, rf bias power of 200 W, pressure of 20 mTorr, HBr of 200 sccm, etching time of 30 s; (g)–(h): Parameters are fixed at rf bias power of 200 W, pressure of 30 mTorr, HBr of 200 sccm, and etching time of 150 s.]

ncreased more rapidly at 80 mTorr than at 10 mTorr. The difference between 10 mTorr and 80 mTorr was more pronounced for the higher Ge concentrations.

Figures 4(a)–4(h) show the vertical profiles of the poly-SiGe gates for the various Ge concentrations and the various process parameters for ICP etching. As shown in Figs. 4(c) and 4(d), when the Ge concentration was above 30%, notching was observed. Almost no notching was observed in Figs. 4(a) and 4(b) for the poly-Si gate and the poly-SiGe gates with the Ge concentration below 30%. More notching was visible with increasing Ge concentration [Figs. 4(a)–4(d)], increasing pressure [Figs. 4(e) to 4(d)], decreasing rf bias Figs. 4(f) to 4(d)], and increasing inductive power [Figs. 4(g) to 4(h)]. Figure 5 shows TEM pictures of the double layered poly-Si/poly-SiGe gate stack of the 100 nm gate line

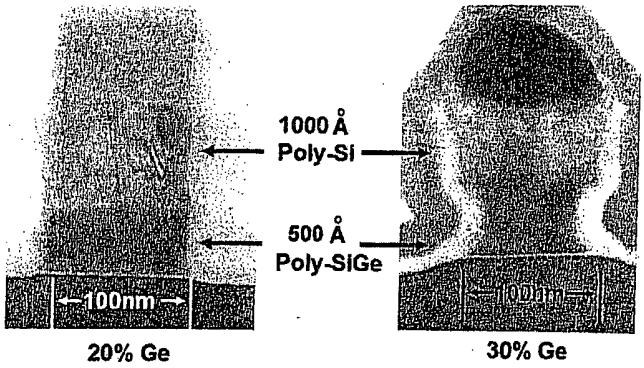


FIG. 5. TEM of etching profiles for gates with linewidth of 100 nm with Ge concentration of 20% and 30%. The thickness is 50 nm for poly-SiGe and 100 nm for poly-Si.

after etching at a condition identical to those in Fig. 4. The notching depth of 50 nm was obtained from poly-SiGe of 30% Ge after the etching for the same period as that for the single layered poly-Si. The clear difference in poly-SiGe gate stack profiles was observed between 20% and 30% Ge.

B. Etching of HfO_2

ICP etching of HfO_2 was carried out using HBr plasmas in the TCP9400SE and using CF_4 plasmas in the ICP2. To compare the etch rates, all other parameters of the plasmas were held constant. Figures 6(a)–6(c) show the HfO_2 etch rates for HBr and CF_4 plasmas, as a function of inductive source power, rf bias power, and pressure. In both HBr and CF_4 plasmas, an increase in the rf bias power or the inductive power resulted in a rapid increase in the HfO_2 etch rate. As the pressure increased, the etch rate of HfO_2 in the HBr plasma decreased, implying that HfO_2 etching depended significantly on ion bombardment. The maximum etch rate of 950 Å/min was obtained in this study at 550 W inductive power, 360 W bias power, and 10 mTorr pressure.

C. Etching of polycrystalline silicon germanium/HfO_2 gate stack

Etching selectivities of poly-SiGe with respect to HfO_2 as a function of rf bias power at 10 mTorr and 80 mTorr are shown in Figs. 7(a) and 7(b), respectively. At 10 mTorr, the etching selectivity decreased as the rf bias power increased [see Fig. 7(a)]. This occurred because the etch rate of HfO_2 increased faster than that of poly-SiGe with increasing the rf bias power. However, the etching selectivities were relatively constant at 80 mTorr [see Fig. 7(b)]. When 8 sccm O_2 was added to 200 sccm HBr at 10 mTorr, the etching selectivity of poly-SiGe to HfO_2 increased significantly due to the lowered etch rate of HfO_2 films. When 8 sccm O_2 was added at 80 mTorr, at the low bias power region the etch rate of HfO_2 films was lowered down to almost 0, and furthermore, at the high bias power region, a significant amount of etching byproducts was deposited to result in net deposition. The occurrence of net deposition was observed by removing the photoresist mask using acetone and by subsequently measur-

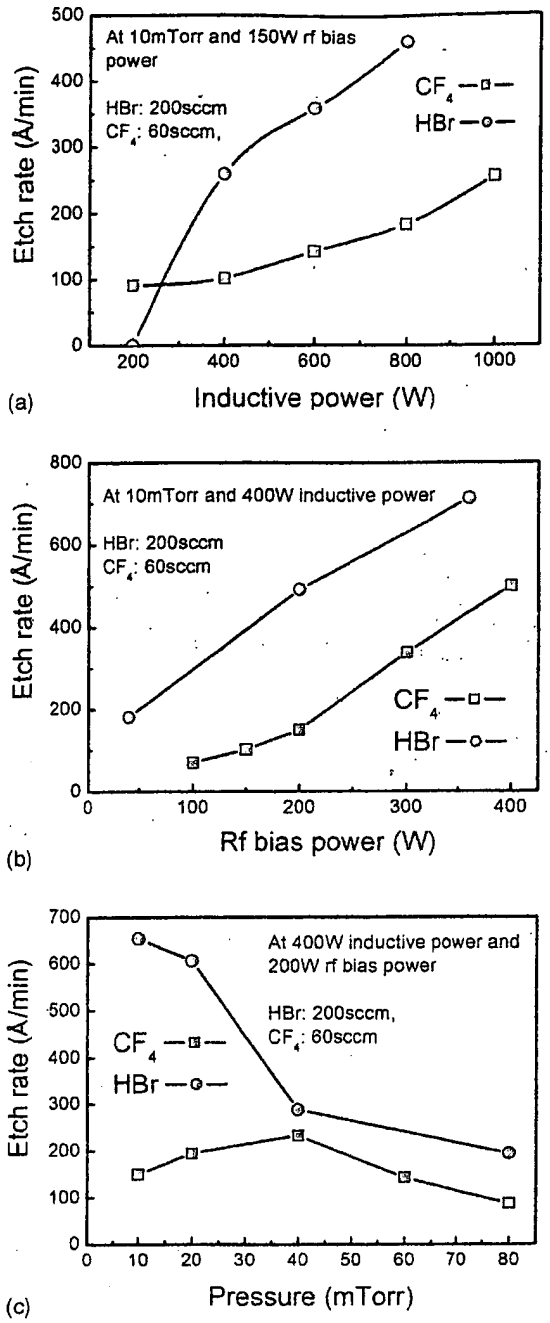


FIG. 6. HfO_2 etch rates in HBr and CF_4 plasmas as a function of (a) inductive power, (b) rf bias power, and (c) pressure. The gas flow was fixed at 200 sccm for HBr and 60 sccm for CF_4. Each experimental condition is: (a) At 10 mTorr pressure and 150 W rf bias power; (b) at 10 mTorr pressure and 400 W inductive power; and (c) at 400 W inductive power and 200 W rf bias power.

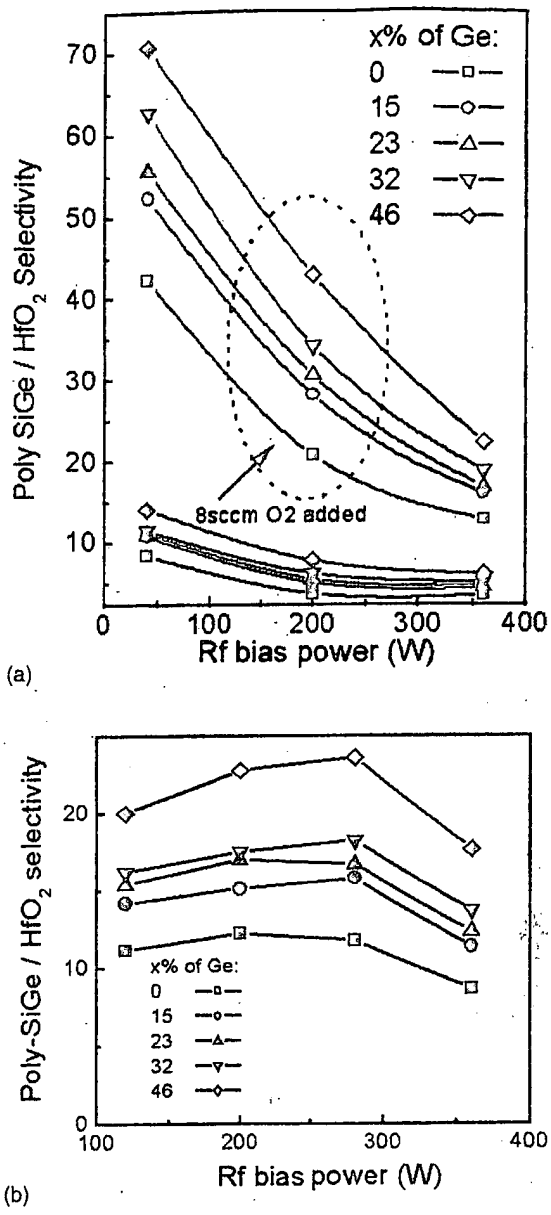
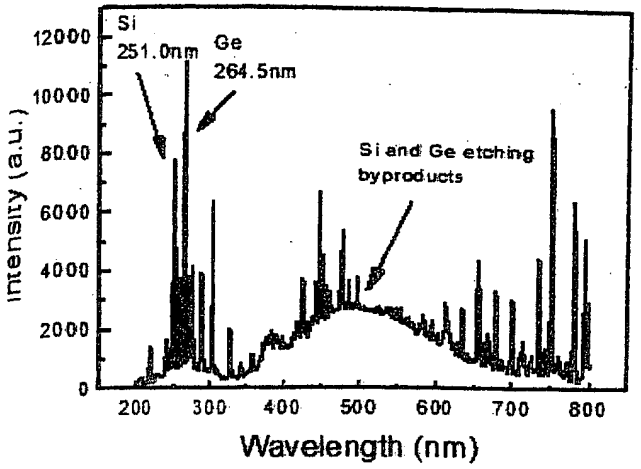


FIG. 7. Poly-SiGe/HfO_2 selectivities as a function of rf bias power at (a) 10 mTorr when pure HBr is used and 8 sccm O_2 is added to HBr, and (b) 80 mTorr when pure HBr is used.

ing step heights between masked areas and unmasked areas of HfO_2 films. The net deposition rate was in the range of 0–40 Å/min.

Figure 8 shows optical emission spectra collected during HBr etching of poly-SiGe. The optical emissions from Si and Ge were detected clearly at the wavelengths of 251.0 nm and 264.5 nm, respectively. We were not able to detect optical emissions generated from Hf atoms, e.g., 307.3 nm, 340.0 nm, 368.2 nm, etc.[19] Furthermore, the optical emissions from the wavelengths of 251 nm (Si) and 264.5 nm (Ge) were used to analyze the temporal change in the etch products generated during ICP etching of the poly-SiGe/HfO_2/Si gate stack in the HBr/Cl_2 plasmas [see Figs. 9(a) and 9(b)]. A multistep etching process was applied to the poly-SiGe/HfO_2/Si gate stack. The oxide breakthrough was performed at the condition of 60 sccm Cl_2, 350 W inductive power, 150 W rf bias power, and 10 mTorr pressure for 10 s. The main etching was performed at the condition of 200 sccm HBr, 350 W inductive power, 135 W rf bias power, and 10 mTorr pressure. Gas flow and pressure were stabilized before each processing step. The result in Fig. 9(a) shows the rapid increase of the Si optical emission peak after etching the gate stack for 80 s, proving that the HfO_2 layer has been removed from the Si substrate. Optical emission results of



G. 8. Optical emission spectra during ICP etching of poly-$Si_{0.54}Ge_{0.46}$ using HBr. Optical emission peaks from Si at 251.0 nm and Ge at 264.5 nm and various etch products from 420 nm to 500 nm are indicated.

e from 264.5 nm [Fig. 9(b)] show that the intensity has ecreased to the noise level after 80 s. It is interesting to bserve from the decrease of the Si peak [Fig. 9(a)] and the ıcrease of the Ge peak [Fig. 9(b)] during the breakthrough eriod, that the Si/Ge ratio in the native oxide of poly-SiGe higher than that in the bulk of poly-SiGe.

I. DISCUSSION

It is interesting to be able to control the amount of the otching from the poly-SiGe gate sidewall by adjusting the ching process parameters. Oehrlein *et al.*[10,20] reported that ıe surface of the poly-SiGe gate structure becomes either Si ch in HBr plasmas or Ge rich in CF_4 and Cl_2 plasmas. ccording to their observation, the SiGe surface resulting om the HBr experiments is expected to be Si rich, and the ıcal disturbance of the Si/Ge ratio at the surface is expected result in more structural defects and thereby more avail-ble electrons. This can explain the development of the otching observed when Ge concentration increases. In addition, deeper notches were obtained from processing conditions where ion energy was reduced, that is, with higher pressure, higher inductive power, and lower rf bias power (see ig. 4). Here, we propose the theory that the notching of the oly-SiGe gates develops when ion energy is insufficient to rm a proper passivation layer on the sidewall in HBr plasmas. Foucher *et al.*[21] reported that the sidewall is passivated y the SiO_x-based layer during poly-Si gate etching in HBr/O_2 plasmas. If the same mechanism is applied to SiGe tching, the etch products are likely to be chemically sputtered by ions and can be the main components of the sidewall passivation layers. Therefore, it is plausible that experimental conditions of higher ion energy can result in thicker assivation layers and the less notching. Notch gates are currently being studied by some researchers[21–23] to develop ort channel devices of gate channel length below 65 nm.

There have been other notching studies in which "footing" was observed as an undesirable phenomenon originating from the conductivity of doped silicon.[24,25] In these reports, the notching occurred during overetching of the poly-Si against the dielectric underlayer when high selectivity between them could be attained. The notching was localized sharply at the interface between the doped poly-Si and the underlying dielectric layer. However, in our observations of Figs. 4 and 5, the controlled notch from poly-SiGe is observed all across the depth of sidewalls, and is similar to "bowing." Considering that the currently studied SiGe gate stack requires a double layer composed of poly-Si on poly-SiGe,[10,26] the notching across the poly-SiGe sidewall may be used for the formation of a T-shaped short channel gate structure.

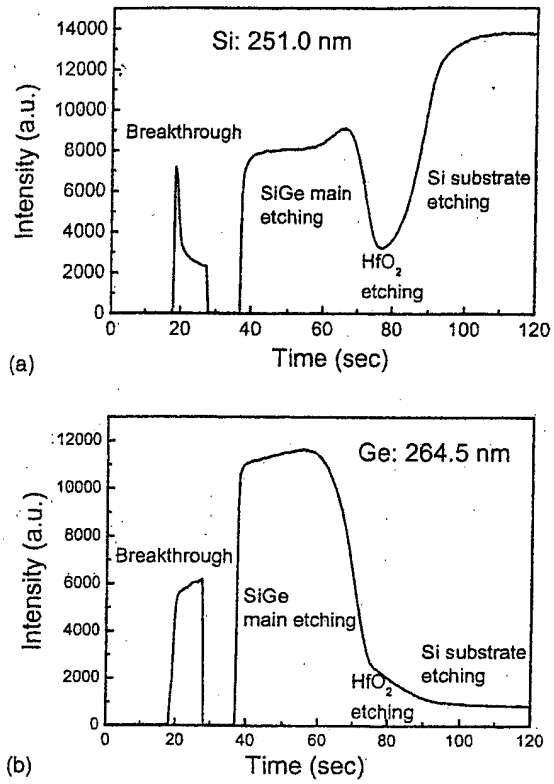


FIG. 9. Optical emission intensity with time during ICP etching of poly-$Si_{0.54}Ge_{0.46}/HfO_2$/Si-substrate gate stack using HBr for (a) Si: wavelength 251.0 nm and (b) Ge: wavelength 264.5 nm.

According to previous observations of high-k dielectrics such as HfO_2, ZrO_2, Al_2O_3, $Ba_{0.5}Sr_{0.5}TiO_3$, and inert electrodes, such as Pt, as potential semiconductor materials,[18,27–32] the etch rates are strongly dependent on ion energy as well as ion density. In ICP etching using inductive power below 1000 W and bias power below 500 W, etch rates were mostly lower than 1000 Å/min, implying that their etching mechanism is predominantly dependent on sputtering by ion bombardment. The universal model for ion bombardment induced etching processes was suggested by Steinbruchel,[33] $Y(E) \approx A(E^{1/2} - E_{th}^{1/2})$, where $Y(E)$ is the sputtering yield at ion energy E, and E_{th} is the threshold ion energy for sputtering. This model predicted the relationship between the etch rate and the ion energy for sputtering dominant etching processes. In Fig. 6(b), we found an approximately linear relation of the etch rates versus rf bias power

during HfO_2 etching. But, we were not able to measure dc bias voltages, because this required a significant modification of our etch system (TCP9400SE). Norasetthekul *et al.*[18] reported that the etching of the sputtered HfO_2 films was not only ion enhanced but also chemically enhanced, showing deviation from the Steinbruchel model. Using another ICP etcher, further studies on the effects of the dc bias voltage are in progress to explore the etching mechanism for various HfO_2 films of different annealing and deposition conditions.

We could sensitively control the etch rates of HfO_2 from HBR/O_2 plasmas. This will be an important method to control the etching selectivity of poly-SiGe with respect to HfO_2. The minimum selectivity requirement of the film to the substrate, $S_{\min}$, is given by[34]

$$S_{\min}=\frac{t_{f,\text{ave}}}{t_{u,\max}}\left[\frac{(1+\alpha)(1+\delta)}{(1-\beta)}-\frac{(1-\alpha)}{(1+\beta)}\right],$$

where $t_{f,\text{ave}}$ is the average film thickness, $t_{u,\max}$ is the maximum allowable consumption of the underlayer, α is the uniformity of film thicknesses, β is the uniformity of etch rates, and δ is the overetching amount. As an example, the advanced gate stack in the 100 nm technology node can consist of a 1500 Å thick poly-SiGe film (thickness uniformity of 3%) and a 30 Å thick HfO_2 underlayer. If overetching up to 50% is allowed in the ICP equipment (with an etch rate uniformity of 3%), we will need to achieve a selectivity of 33 or higher in order to form an advanced gate stack by ICP etching. Considering that the removal rate of the remaining HfO_2 by diluted HF is extremely low, it can be important to remove most of the underlying HfO_2 by plasma etching with very little consumption of Si substrate. This can be done if the selectivity could be very precisely controlled in the neighborhood of 33 as a minimum.

There have been reports on the effects of O_2 addition on the etching selectivity of poly-Si to SiO_2.[35–37] The results from HBr/O_2 plasmas[35] showed that the poly-Si surface could be extensively oxidized with O_2 less than 2%, and the poly-Si etching rates and, therefore, the etching selectivities could be lowered accordingly. On the other hand, the results from Cl_2/O_2 plasmas[36] showed that the O_2 addition barely affected the poly-Si etch rates but lowered the SiO_2 etch rates via etch-deposition competition, and this resulted in the higher etching selectivity. In our results of Fig. 7, the etching selectivity of poly-SiGe to HfO_2 increased significantly with the introduction of 3.8% O_2 in HBr. The results from Fig. 7(a) demonstrate that the etching selectivity could be sensitively controlled by changing the rf bias power in the presence of a small amount of oxygen. We noticed from our preliminary XPS analysis that the change in the selectivity might be mainly due to the change in the film property of the HfO_2 underlayer. When O_2 is added to HBr, it dissociates quickly in the plasma to react with nonvolatile Hf or Hf etch products to form HfO_x or HfO_xBr_y, nullifying the etching of HfO_2 by HBr. We propose that, as the etching is carried out, the surface of the HfO_2 film becomes richer in Hf by a preferential etching process for O, but it can quickly return to HfO_x when a certain amount of reactive O is available from the plasma. The precise addition of O_2 is critical in controlling removal rates of HfO_2 and thereby etching selectivities. According to this model, the processing window can be determined by competition between low selectivity from high etch rates of HfO_2 without O_2 and high selectivity from *in situ* reformation of HfO_2 with O_2.

V. CONCLUSIONS

We were able to control the amount of notching that was formed by ICP etching of poly-SiGe, and to form a notch gate that can be used for short channel devices of a gate length smaller than 65 nm. Notching was controlled by varying the etching process parameters of inductive power, rf bias power, and pressure, as well as by varying the Ge concentration in poly-SiGe. Notching became more pronounced in the conditions where ion energy was reduced. Etching of HfO_2 was strongly dependent on the sputtering by ion bombardment. By controlling the etching selectivity of poly-SiGe to HfO_2 with the change in the rf bias power in the presence of a small amount of O in HBr plasmas, we were able to demonstrate the processing feasibility of the formation of a poly-SiGe/HfO_2 gate stack using ICP etching.

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